REMARKS

Claims 1-17 were pending in the above-identified application and are amended as indicated above. The claim amendments correct typographical errors and clarify the claim language but are not intended to limit the scope of the claims.

Claims 1-4, 6, and 9-13 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,668,815 (Gittinger). Applicants respectfully traverse the rejection.

Gittinger is directed to using direct memory access (DMA) circuitry for testing of an internal memory in a microcontroller. In particular, Fig. 1 of Gittinger shows a microcontroller 10 including DMA control 20 and internal memory 30. Microcontroller 10 also includes an internal bus 34 that is connected to DMA control 20, internal memory 30, a processor core 16, and a bus interface 32. For a test operation, Gittinger describes setting up DMA control 20 for DMA operations that write and read to internal memory. Bus interface 32, which is connected to an external bus 36, can be operated in a "show read" to allow a tester 42 to evaluate whether the read data has the desired values. See Gittinger, beginning at column 6, line 40.

Independent claim 1 distinguishes over Gittinger at least by reciting, "an internal memory containing test routines that the processing core executes to test the integrated circuit." Gittinger fails to suggest an internal memory containing test routines. For example, beginning at column 9, line 30, Gittinger states, "sets of test vectors are created to perform defect testing upon internal memory 30 (i.e. BIST). The test vectors comprise feeding instructions to processor core 16 via external bus 36. These instructions initialize configuration registers within processor core 16, initialize DMA controller 10, and initiate the DMA transfers by asserting a PIO pin coupled to the DMA request pins." Gittinger thus teaches instructions fed from an external source (e.g., a tester 42) to configure the DMA operation, but fails to disclose "an internal memory containing test routines that the processing core executes to test the integrated circuit" as recited in claim 1.

Claim 1 further distinguishes over Gittinger by reciting, "an interface coupled to the processing core to permit activation of a first output signal indicating a test result from executing the test routines." In regard to this element, the Examiner cited interface 44, which is shown in Fig. 2 of Gittinger. However, Gittinger beginning at column 8, line 67 describes that "Typically, tester 42 and test interface 44 are sold together as a unit. Test interface 44 is used to contact with microcontroller 10, and is generally customized for each integrated circuit which tester 42 is used to test." Accordingly, Gittinger does not indicate or suggest that interface 44 is an element of the integrated circuit being tested.

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Further, Gittinger fails to suggest "activation of a first output signal indicating a test result from executing the test routines." As noted above, the instructions that processor core 16 executes for testing configure DMA control 20. Tester 42 can then activate DMA operations via external pins 46, 48, and 50, while processor core 16 waits. (See, for example, the paragraph beginning at column 14, line 4 of Gittinger.) The resulting DMA operations output data read from internal memory 30, and tester 42 can evaluate the data to determine a test result. Accordingly, Gittinger discloses output from microprocessor 10 from a DMA operation, not a signal indicating a test result from executing test routines.

Claim 1 and claims 2-4 and 6, which depend from claim 1, are thus believed patentable over Gittinger.

Claim 3 further distinguishes over Gittinger by reciting, "a first terminal on which the processing core activates the first output signal to indicate the test result; and a second terminal on which the processing core activates a second output signal to indicate when the first output signal indicates the test result." As noted above, Gittinger discloses DMA output of data, not processor core activation of a result signal. Gittinger further fails to suggest use of a pair of terminals as recited in claim 3.

Claim 4 further distinguishes over Gittinger by reciting, "the processor toggles the first output signal to verify that the first output signal is functional."

Independent claim 9 distinguishes over Gittinger at least by reciting, "using a processing core in the integrated circuit to execute test routines stored in the integrated circuit. As noted above, Gittinger fails to disclose storing test routines in the integrated circuit being tested.

Claim 9 further distinguishes over Gittinger by reciting, "observing a first signal output from the integrated circuit as a result of the processing core executing the test routines, the first signal indicating whether the execution of the test routines detected a failure in the integrated circuit." As noted above, Gittinger discloses outputting data during a DMA operation, and an external tester (not internally executed test routines) is responsible for detecting an error in the data.

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Claim 9 and claims 10-13, which depend from claim 9, are thus patentable over Gittinger.

Dependent claims 10-13 further distinguish from Gittinger by reciting uses of further signals from the integrated circuit that are neither disclosed nor suggested in Gittinger.

For the above reasons, Applicants request reconsideration and withdrawal of the

rejection under 35 U.S.C. § 102.

Claims 5, 7, 8, and 14-17 were rejected under 35 U.S.C. § 103(a) as unpatentable over Gittinger in view of related art described on pages 1 and 2 of Applicants' specification. Applicants respectfully traverse the rejection.

Claims 5, 7, and 8 and claims 14-17 respectively depend from independent claims 1 and 9, which are patentable over Gittinger for the reasons given above. Since Applicants discussion of the related does not provide the elements of claims 1 and 9 that are missing from Gittinger, claims 5, 7, 8, and 14-17 are patentable over the combination of Gittinger and Applicants' description of related art for at least the same reasons provided above in regards to the rejection under 35 U.S.C. § 102.

Claim 7 further distinguishes over Gittinger by reciting, "the internal memory contains a first set of test routines for execution during a production test of the integrated circuit and a second set of test routines for execution during an in-product test of the integrated circuit." The Office Action starting at page 3, line 15 indicates that Gittinger does not disclose "that the internal memory contains a first set of test routines for execution during a production test ... and a second set of test routines for execution during an in-product test... However, the admitted prior art (Pgs. 1-2) does disclose that the internal memory contains a first set of test routines for execution during a production test ... and a second set of test routines for execution during an in-product test." Applicants respectfully disagree with the Examiner's interpretation of Applicants' discussion of the related art.

Paragraph **[0004]** of Applicants' specification describes a situation where "ASICs need at least two types of tests, a test implemented with an external tester and a built-in self-test (BIST) that the ASIC performs in a product." Paragraph **[0005]** of Applicants' specification states, "BIST tests are generally implemented using special BIST logic that applies deterministic signal patterns in an attempt to exercise the logic paths." This description is of production testing controlled by a tester and in-product testing control by BIST logic. Applicants' discussion of the related art nowhere indicates that any related art stored test routines of any kind in internal memory.

For the above reasons, Applicants request reconsideration and withdrawal of the rejection under 35 U.S.C. § 103.

In summary, claims 1-17 were pending in the application. Claims 10 and 12 are amended to correct typographical errors. For the above reasons, Applicants respectfully

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request allowance of the application including claims 1-17.

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